CARTONI

PROFESSIONAL CAMERA SUPPORT

SUPPORTS YOUR VISION

Encoded Head user manual

Version 2018/08/31

Summary

Encoded head

The latest response to encoded support as needed in the Virtual Reality shooting. Strong, versatile, including all features of a standard CARTONI fluid action camera support head, the encoded heads features extremely high resolution direct sensing encoders in both pan and tilt, absolute positioning with no need to re-calibrate at start up, simple cabling.

CARTONI encoded heads are compatible with most 3D packages for real time camera/scene movement in virtual set and pre-visualization, it is the ideal solution for sports 3D graphic insertions.

Tech Specs

Operating temperature	$-15°C \div +85°C$
Storage temperature	$-15°C \div +120°C$
Supply voltage	$Dc\ 5V \pm\ 10\%$
Current w/o load typ.	$100mA$
Encoder resolution	$22bit\ (4.194.304\ Count/Revolution)$
Output code	$BiSS - C$
Drives	$Clock\ and\ Data\ RS422\ levels$
3dB limiting frequency	$500\ kHz$
Absolute accuracy	$\pm\ 35''$
Repeatability	$\pm 10''$

Electrical connections

Pan/Tilt encoders

Lemo ECG.1B.307.CLL

1	GND	
2	Not Used	
3	+5V	
4	Data	Input
5	Data/	Input
6	Clock	Output
7	Clock/	Output

BiSS

Electrical Data

Input / Output Signal

$Clock\ and\ \overline{Clock}$:	$RS422\ (Input)$
$Data\ and\ \overline{Data}$:	$RS422\ (Outout)$
$Clock\ frequency$:	$100kHz \dots 10MHz$
$Timeout_{SENS}$[1]:	$12\mu s$
$Timeout_{reg}$:	$51\mu s$

Outputs:

Driver output current:	$\max 60\ mA$
Short circuit output current :	$\pm\ 250\ mA$

Cable:

Leads for clock and data should be twisted in pairs
Entire cable shielded and according to CAT 5
Cable capacity $\leq 100\ pF/m$
Cable length $\max 100\ m$
Baud rate $< 10\ MHz$

[1] $Timeout_{SENS}$ and $timeout_{reg}$ are programmable.

BiSS Protocol

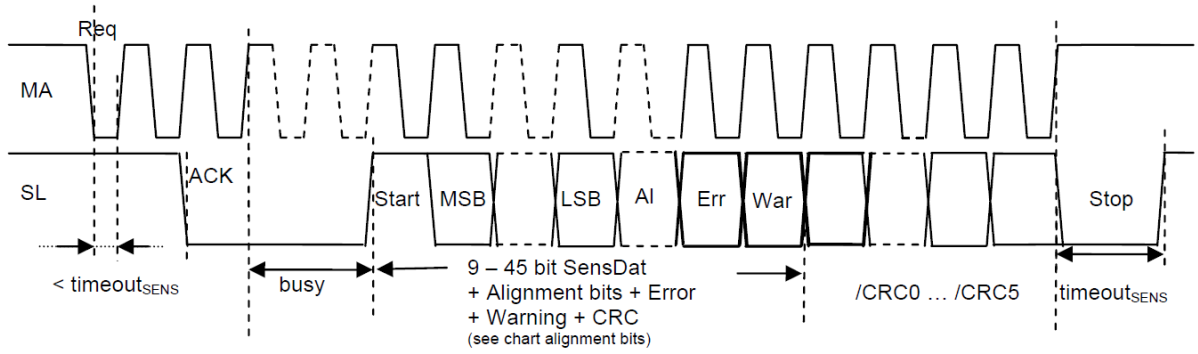
Bidirectional Serial Sensor Interface (BiSS)

The Serial BiSS communication differentiates between the fast transmission of sensor data and the slower transmission of register data. The transmission of sensor data is unidirectional; here, encoder can only output data, whereas the bidirectional transmission of register data can include read and write access.

The BiSS sensor interface can be operated in an SSI compatible mode, in which only a lower transmission speed is possible and encoder may not demand processing time for procedures such as interpolation, for example.

Transmitting sensor data (BiSS-Mode)

Transmission is initiated by a falling edge on the master line (MA). The master then again ramps the master line up to high within a stipulated period (<timeout$_{SENS}$) and continues the clock pulse. encoder acknowledges the request for sensor data on the second rising MA edge with a low signal at SLO (see description of the BiSS protocol). The next rising edge gives the validity of the position data and is interpreted as a start bit by the master.
Depending on the configuration the length of encoder's position data varies between 9 and 45 bits, plus an error bit and a warning bit. With a maximum length of 47 bits this data is protected by a 6-bit cyclic redundancy check value or CRC (polynomial 0x43 = "1000011b") which directly follows the data. **MCD: Multicycle data is not supported!**



Transmission of sensor data in BiSS mode.

The Warning – Bit (War) is coupled to the internal temperature sensor of the OptoAsic. It is high, when the following temperature limits are exceeded or under - run:

Operating temperature	Internal Warning tresholds
- 15° ... +120°C	-20° .. +125°C

The Error – Bit (Err) is coupled to the LED – current. It is high, when an factory defined threshold is exceeded. An excess LED current can indicate Pollution; Condensation, Over temperature or Ageing of the LED

Chart: Alignment Bits

MT	ST	Alignment Bits
0	9	0
12	10	0
16	11	0
20	12	0
24	13	0
	14	0
	15	2
	16	1
	17	0
	18	6
	19	5
	20	4
	21	3
	22	2
	23	1
	24	0

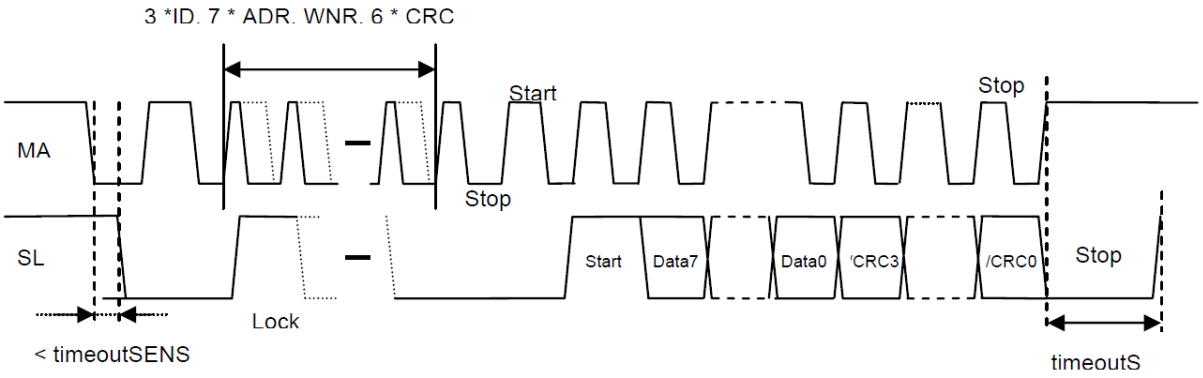
Values in columns: **“Length of Data bits”**

Register – mode (BiSS – Interface)

The register communication is initiated by a low signal following the first falling edge from the master on the clock line. The master keeps the clock line on low until the encoder reacts with a falling edge on the data line and thus signaled the changeover to register mode. After this has happened the master transmits the addressing data coded as a PWM signal (pulse width modulated clock signal). The individual sensors (slaves) are addressed by slave IDs which are generated automatically according to the order of the slaves in the sequential circuit. encoder uses two slave Ids (e.g. ID "000" and "001") so that it can extend the available addressing range from 7 to 8 bits.

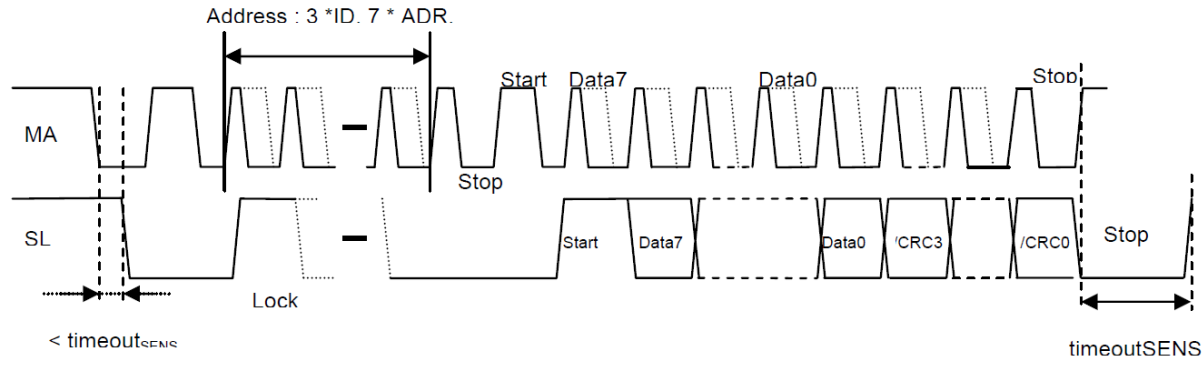
Register mode: read

Once encoder has signaled the changeover to register mode the master transmits the start bit, the 3- bit slave ID and the 7-bit register address for the addressing sequence, followed by the WNR bit ("0") and the 6-bit CRC. Each bit is coded by the duty cycle (PWM), including the start bit. The generator polynomial for the 4-bit CRC is 0x13 = "10011" (see the definitions in the description of the BiSS protocol). The encoder does not require any processing time to read the internal registers and answers immediately with the data of the addressed registers. When reading the external EEPROM registers the output is delayed until the data from the EEPROM has been made available. All 8-bit read data can also be checked for transmission errors by the 4-bit CRC 0x13.



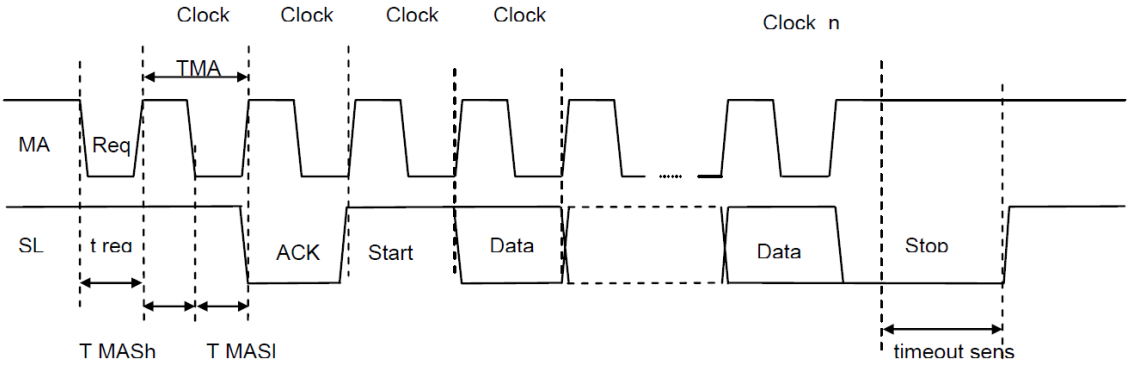
Register mode: write

When data is being written to a register, after the encoder has confirmed the mode changeover the same addressing sequence as for read access is used (with the WNR bit at "1"). Following the second start bit the master transmits the data to be written which encoder returns for verification, bit by bit one clock pulse later. As in the above, a 4-bit CRC have to follow the 8-bit write data which is returned by encoder in the same manner, however not in PWM format. A transfer to the EEPROM registers is processed in the background and can be validated by a read access once transmission is over.



Timing

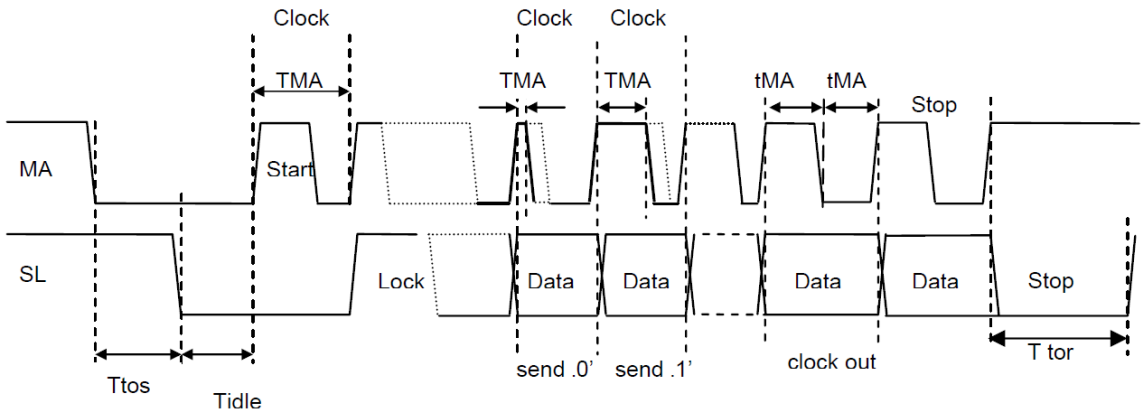
Timing BiSS Sensor Mode



BiSS Sensor Mode						
Symbol	Parameter	Conditions	min	typ	max.	Unit
timeout sens (Ttos)[2]			9,9	12,4	14,9	µs
TMAS	Permissible Clock Period		100 ns		2* Ttos	
tMASh	Clock Signal Hi Level Duration		50		Ttos	ns
tMASl	Clock Signal Lo Level Duration		50		Ttos	ns
Treq	Data Request Lo Level Duration	only with SAR converter	50		Ttos	ns

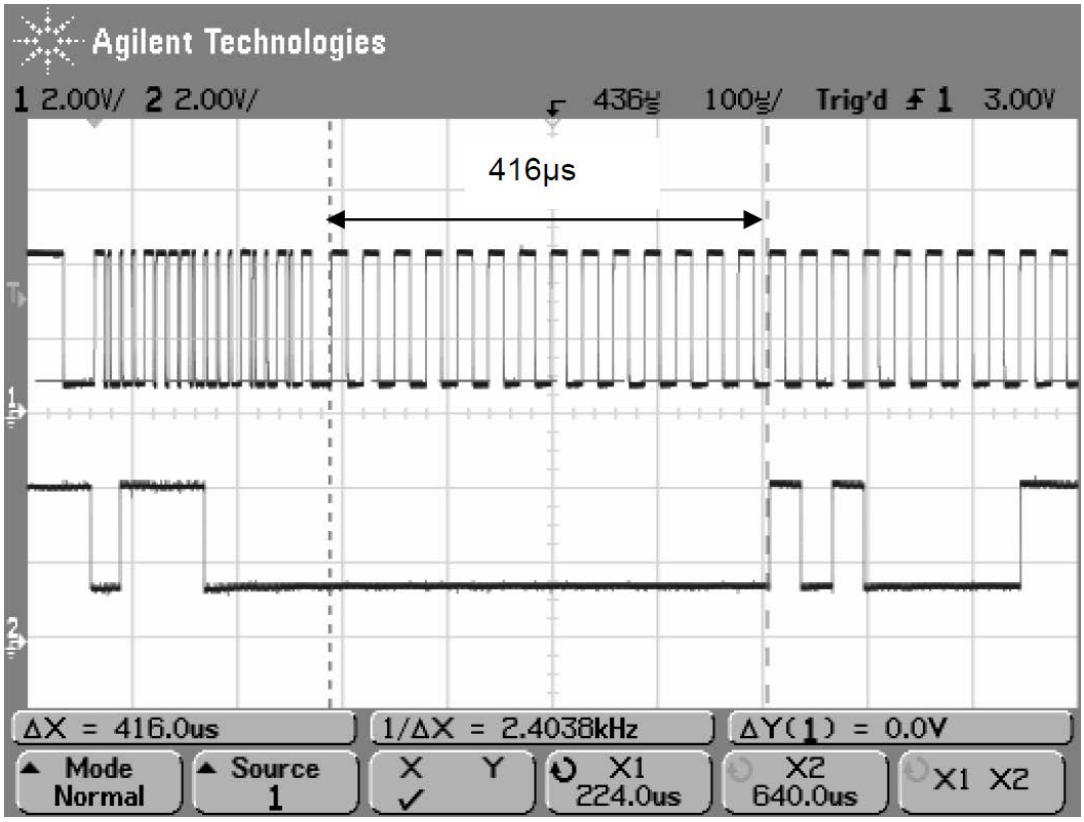
[2] Ttos = is programmable Time

Timing BiSS Register Mode



BiSS Register Mode					
Symbol	Parameter	Conditions	Min	Max.	Unit
TMAR	Permissible Clock Period	CFGTOR = 2Eh	4	52	µs
Tidle	Permissible Clock Halt (idle)		0	Indefinite	
tMARh	Clock Signal Hi Level Duration	read out of register data	50 %		% TMAR
tMARl	Clock Signal Lo Level Duration			Ttor	ns
tMA0h	.Logic 0" Hi Level Duration		10	30	% TMAR
tMA1h	.Logic 1" Hi Level Duration		70	90	% TMAR

Example for read register 78h
Keep clock active until start bit is sent by encoder. Approx. time ~ 416 µs



See Figure: The clock should be applied until encoder sends ACK (~ 416 µs). This time is needed because the ASIC has to read the EEPROM internally before sending the data. There are different times for different registers because registers are mapped either directly in the ASIC or externally to an EEPROM value (takes more time).